

REMARKS

Claims 1-15 remain pending in the application. Reconsideration of the application is requested.

Claims 1-15 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Appropriate amendments have been made to the claims as indicated above to address the Section 112 issues. Applicant submits that these amendments merely clarify that which was already claimed and do not narrow the scope of the claims.

Claims 12-14 were rejected under 35 U.S.C. 102(e) as being anticipated by Miyanaga.

The Miyanaga reference has an effective date under Section 102(e) of July 2, 2003 (i.e., its 35 U.S.C. 111(a) filing date claiming priority to the Japanese application) (see, for example, MPEP 706.02(f)(1), example 3). Pursuant to MPEP 706.02(b), a rejection based on 35 U.S.C. 102(e) can be overcome by (E) perfecting a claim to priority under 35 U.S.C. 119(a)-(d). Applicant has done so in this case and shown a foreign filing priority date of December 2002 which antedates the July 2003 effective prior art date of the Miyanaga reference. Thus, the Examiner cannot rely on Miyanaga in rejecting claims 12-14.

Notwithstanding the foregoing, Applicant submits that Claim 12 is patentable over Miyanaga because the reference fails to teach each and every limitation of the claimed invention. The Office Action fails to show which features of Miyanaga meet the specifically claimed structural limitations recited in claim 12. The rejection accordingly is deficient as the Examiner has failed to show the pertinence of the reference and clearly explain the basis for the rejection (see, for example, 37 CFR 1.104(c)(2)).

Further notwithstanding the foregoing, Claims 13-14, as amended to overcome the Section 112 rejection, are believed to be patentable over Miyanaga because this reference fails to teach or suggest overriding the sensing of the output regulated voltage to sense a higher voltage. This claim limitation is similar in scope to limitations present in allowed claim 1 (“increases the sensed output voltage as the current through the current sense transistor exceeds the reference current value”) and claim 5 (“increases the sensed regulator output voltage if the sensed current exceeds the reference current”).

In view of the foregoing, Applicants respectfully submit that the application is in condition for favorable action and allowance.

Respectfully submitted,
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